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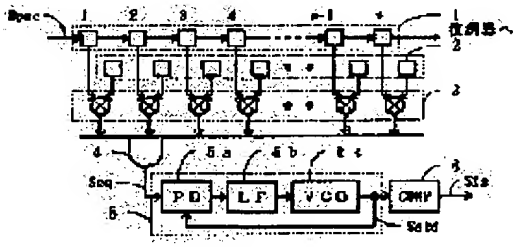
(54) FRAME SYNCHRONIZATION DETECTION CIRCUIT

(57)Abstract:

PURPOSE: To prevent the missing of a frame synchronization detection signal by an error in a frame synchronization code by comparing a phase of a coincidence signal from an n-input AND circuit with a phase of a reference signal so as to control an oscillated frequency of the reference signal based on a difference signal.



CONSTITUTION: An EX-OR circuit 3 compares the frame synchronizing signal of the data signal Dpac of a packet structure received by the n-stage of shift registers 1 with a frame synchronizing signal stored in advance in n-stages of 1-bit memories 2 one by one bit each. When all bits are coincident, the phase of the coincidence signal Seq outputted from an n-input AND circuit 4 is compared with the phase of the reference signal of a voltage controlled oscillator 5c by a PLL circuit 5, and a difference signal controls the oscillated frequency of the reference signal to generate a reference signal Ssta with a stable oscillating frequency. Then a waveform generating section 6 is used to shape the reference signal with a prescribed waveform

and provides the output of a frame synchronization detection signal Sfs. Thus, even when error data of a frame synchronization code are received, the synchronization is stable detected.